REMARKS

This application is a divisional application of U.S. Patent Application Serial No. 09/388,856 and is being filed responsive to a restriction requirement therein. Accordingly, claims 18-36 have been canceled without prejudice. Claims 1-17 and 37-49 remain in the application for consideration.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

This application is believed to be in condition for allowance and action to that end is requested. The Examiner is requested to telephone the undersigned in the event that the next office action is one other than a Notice of Allowance. The undersigned is available during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: May 3, 2001

By: _____

Frederick M. Fliegel, Ph.D.
Reg. No. 36,138

Version with markings to show changes made.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/388,856
Priority Filing Date .....September 1, 1999
Inventor .....Luan C. Tran
Assignee..... Micron Technology, Inc.
Priority Group Art Unit 2813
Priority Examiner .....L. Schillinger
Attorney's Docket No. MI22-1689
Title: Semiconductor Processing Methods of Forming Integrated Circuitry

37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii) FILING REQUIREMENTS TO ACCOMPANY PRELIMINARY AMENDMENT

Deletions are bracketed, additions are underlined.

In the Specification

At page 1, after the title insert:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Divisional Application of U.S. Patent Application Serial No. 09/388,856, filed on September 1, 1999, entitled "Semiconductor Processing Methods of Forming Integrated Circuitry" and naming Luan C. Tran as inventor.

In the Claims

Claims 18-36 have been canceled without prejudice.

Claims 5, 16 and 45 have been amended as shown below.

5. (Amended) [In a common] A semiconductor processing method comprising:

a masking step providing a common mask; and [in]

[a common] an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages.

16. (Amended) [In a common] A semiconductor processing method comprising:

a [common] masking step providing a common mask; and [in]

[a common] an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages, at least some of the devices forming memory access devices.

45. (Amended) The method [ov] of claim 41 wherein the storage node side of the memory access device is masked from the halo implant.

END OF DOCUMENT